An integer instruction set architecture and implementation

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Abstract of **TW 497074 (B)**
The present invention is directed to a processor element, such as a microprocessor or a micro-controller, structured to execute an integer instruction set architecture. In a specific embodiment, the present invention provides a method for loading an arbitrary constant number into a memory location, through a series of immediate integer instructions. In another specific embodiment present invention provides a method for normalizing a number. The method includes: counting a total number of sign bits in the binary number and then determining a result by subtracting one from the total number. The result may be used for normalizing a number by left-shifting the binary number by the result.

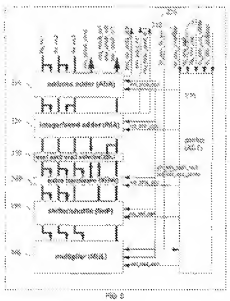

Fig 8

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